REMARKS

Claims 12, 15-17, 20-22, 25-27, 30 and 31 are pending in the present application. Claims 12, 17, 22 and 27 have been amended. Claims 14, 19, 24, and 29 have been canceled.

Claim Rejections – 35 U.S.C. 102/103

Claims 12, 14, 15, 17, 19, 20, 22, 24, 25, 27, 29 and 30 have been rejected under 35 U.S.C. 103(a) as being obvious over the Elenius et al. reference (U.S. Patent No. 6,441,487) in view of the Hashimoto reference (WO 98-25297), the Matsumoto reference (Japanese Patent Publication No. 5-234972) and the Yamada reference (U.S. Patent No. 6,048,749). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

It is noted that the Examiner has not cited of record or relied upon the Hashimoto reference (U.S. Patent No. 6,475,896) in this rejection. Accordingly, the comments as follows are presented in view of the non-English language Hashimoto reference (WO 98-25297), which has been provided by the Examiner as including merely an English language abstract.

The semiconductor device of claim 12 includes in combination among other features a protective layer "made of polymide resin on the second surface of the semiconductor element,... wherein the protective layer is a peelably removable UV sensitive tape comprised of a hardened synthetic resin that bonds the tape to the

second surface of the semiconductor element". Applicant respectfully submits that claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

As noted above, the semiconductor device of claim 12 includes a protective layer that is peelably removable UV sensitive tape, that is made of polymide resin and that is on the second surface of the semiconductor element. The second surface of the semiconductor element is opposite the first surface of the semiconductor element, wherein the first surface of the semiconductor element has an electrode, a wiring portion, a conductive post, a resin layer and an external connection thereon. The protective layer of claim 12 that is peelably removable UV sensitive tape, that is made of polymide resin and that is on the second surface of the semiconductor element, inhibits reflex of the semiconductor element.

The primarily relied upon Elenius et al. reference as shown in Fig. 2 includes an organic protective coating 34 on the rear surface 16 of wafer 14. The primarily relied upon Elenius et al. reference does not disclose a protective layer that is a peelably removable UV sensitive tape on a second surface of a semiconductor element, as would be necessary to meet the features of claim 12. The Elenius et al. reference does not inhibit reflex of semiconductor wafer 14.

The secondarily relied upon Hashimoto reference (WO 98-25297) does not disclose a protective layer that is peelably removable UV sensitive tape made of polymide resin on a second surface of a semiconductor element, as would be

necessary to meet the features of claim 12. In particular, the English language abstract of the foreign language Hashimoto reference (WO 98-25297) merely describes in general a resin layer 14 on an upper or first surface of wafer 10 that includes circuit elements. Resin layer 14 of the Hashimoto reference is not on a second surface of wafer 10.

The secondarily relied upon Yamada reference teaches in column 1, lines 27-39 that to prevent damaging a semiconductor wafer from cracking at the time of grinding, it is commonly practiced to protect the front surface of the wafer where the semiconductor devices are formed, by an adhesive medium such as an adhesive tape. The Yamada reference does not disclose a protective layer that is a peelably removable UV sensitive tape made of a polymide resin on a second surface of a semiconductor element, as would be necessary to meet the features of claim 12.

The English abstract of the Matsumoto reference generally describes an adhesive tape stuck to the rear surface of a wafer. The Matsumoto reference does not disclose a protective layer that is a peelably removable UV sensitive tape made by polymide resin on a second surface of a semiconductor element, as would be necessary to meet the features of claim 12. The prior art as relied upon by the Examiner taken together does not disclose the use of a peelably removable UV sensitive tape made of polymide resin on a second surface of a semiconductor element, and thus does not make obvious the features of claim 12. Accordingly, Applicant respectfully submits that the semiconductor device of claim 12 would not

have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 12 and 15, is improper for at least these reasons.

The semiconductor device of independent claim 17 includes in combination among other features a protective layer "made of polymide resin on the second surface of the semiconductor element,...wherein the protective layer is a peelably removable UV sensitive tape which comprises a hardened synthetic resin that bonds the tape to the second surface of the semiconductor element". Independent claims 22 and 27 respectively include similar features. Applicant respectfully submit that the semiconductor devices of respective claims 17, 22 and 27 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 17, 20, 22, 25, 27 and 30, is improper for at least somewhat similar reasons as set forth above with respect to claim 12.

Claims 12, 14-17, 19-22, 24-27 and 29-31 have been rejected under 35 U.S.C. 103(e) as being unpatentable over Applicant's admitted prior art (AAPA) in view of the Elenius et al., Hashimoto, Matsumoto and Yamada references. Applicant respectfully submits that Applicant's admitted prior art Fig. 4 does not overcome the above noted deficiencies of the previously relied upon Elenius et al., Hashimoto, Matsumoto and Yamada references. Accordingly, Applicant respectfully submits that this rejection is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to July 14, 2008, for the period in which to file a response to the outstanding Office Action. The required fee of $460.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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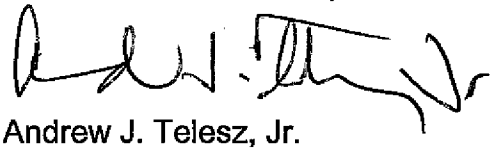

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